

## PRECISION VOLTAGE REGULATOR

### DESCRIPTION

This monolithic voltage regulator is designed for use with either positive or negative supplies as a series, shunt, switching, or floating regulator with currents up to 150mA. Higher current requirements may be accommodated through the use of external NPN or PNP power transistors. This device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor, current limit, and remote shutdown circuitry.

The SG723 will operate over the full military ambient temperature range of -55°C to 125°C.

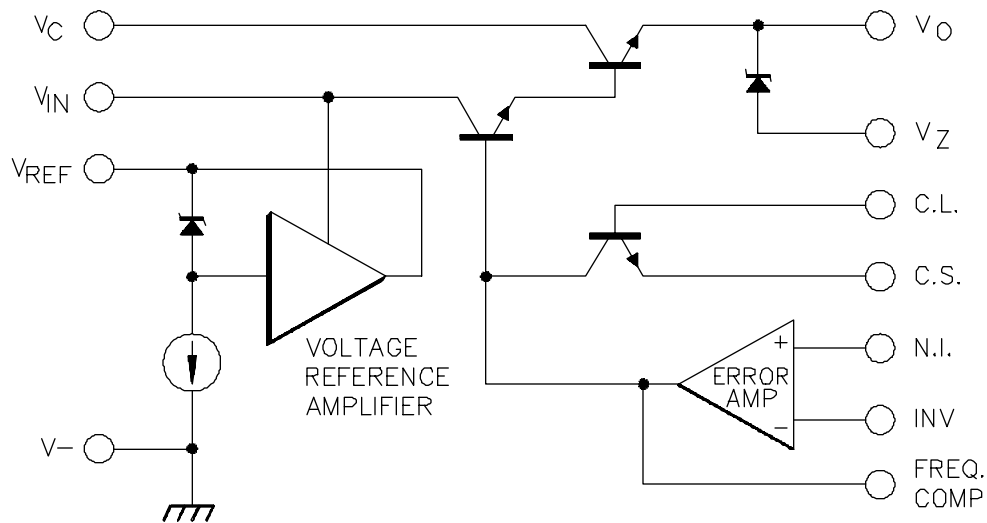
### FEATURES

- Positive or negative supply operation
- Series, shunt, switching or floating operation
- Low line and load regulation
- Output adjustable from 2V to 37V
- Output current to 150 mA
- Low standby current drain
- 0.002%/°C average temperature variation

### HIGH RELIABILITY FEATURES - SG723

- ◆ Available to MIL-STD-883 and DESC SMD
- ◆ MIL-M38510/10201BHA - JAN 723F
- ◆ MIL-M38510/10201BIA - JAN 723T
- ◆ MIL-M38510/10201BCA - JAN723J
- ◆ Radiation data available
- ◆ LMI level "S" processing available

### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS (Note 1)

Pulse (50 ms) Input Voltage from $V_{IN}$ to $V_-$ .....	50V
Continuous Input Voltage from $V_{IN}$ to $V_-$ .....	40V
Input to Output Voltage Differential .....	40V
Maximum Output Current .....	150mA
Current from $V_z$ (J-Package only).....	25 mA

Current from $V_{REF}$ .....	15mA
Operating Junction Temperature	
Hermetic (T, J, F, L-Packages).....	150°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) .....	300°C

Note 1. Exceeding these ratings could cause damage to the device.

## THERMAL DATA

J Package:

Thermal Resistance-Junction to Case, $\theta_{JC}$ .....	30°C/W
Thermal Resistance-Junction to Ambient, $\theta_{JA}$ .....	80°C/W

T Package:

Thermal Resistance-Junction to Case, $\theta_{JC}$ .....	25°C/W
Thermal Resistance-Junction to Ambient, $\theta_{JA}$ .....	130°C/W

F Package:

Thermal Resistance-Junction to Case, $\theta_{JC}$ .....	80°C/W
Thermal Resistance-Junction to Ambient, $\theta_{JA}$ .....	145°C/W

L Package:

Thermal Resistance-Junction to Case, $\theta_{JC}$ .....	35°C/W
Thermal Resistance-Junction to Ambient, $\theta_{JA}$ .....	120°C/W

Note A. Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ .

Note B. The above numbers for  $\theta_{JC}$  are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The  $\theta_{JA}$  numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

## RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage Range .....	( $V_{OUT} + 4.5V$ ) to 38 V
Output Current Range .....	5mA to 45mA
Reference Current.....	5mA

Zener Current (J-Package only).....	5mA
Operating Ambient Temperature Range	
SG723 .....	-55°C to 125°C

Note 2. Range over which the device is functional.

## ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply for the operating ambient temperature of  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_C = 12V$ ,  $V_- = 0V$ ,  $V_{OUT} = 5V$ ,  $I_L = 1\text{ mA}$ ,  $R_{SC} = 0\Omega$ ,  $C_1 = 100\text{pF}$ , and divider impedance as seen by error amplifier  $\leq 10\text{K}\Omega$ . Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG723			Units
		Min.	Typ.	Max.	
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input to Output Differential		3.0		38	V
Line Regulation (Note 3)	$V_{IN} = 12V$ to $15V$ $T_A = T_{MIN}$ to $T_{MAX}$		0.01	0.1	% $V_{OUT}$
				0.3	% $V_{OUT}$
Load Regulation (Note 3)	$V_{IN} = 12V$ to $40V$ $I_L = 1$ to $50\text{ mA}$ $T_A = T_{MIN}$ to $T_{MAX}$		0.02	0.2	% $V_{OUT}$
			0.03	0.15	% $V_{OUT}$
				0.6	% $V_{OUT}$
Ripple Rejection	$f = 50\text{ Hz}$ to $10\text{KHz}$ $C_{REF} = 0$		74		dB
	$C_{REF} = 5\mu\text{F}$		86		dB
Temperature Stability (Note 4)	$T_A = T_{MIN}$ to $T_{MAX}$		0.002	0.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\Omega$		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	$BW = 100\text{Hz}$ to $10\text{KHz}$ $C_{REF} = 0$		20		$\mu\text{V}_{rms}$
	$C_{REF} = 5\mu\text{F}$		2.5		$\mu\text{V}_{rms}$
Standby Current Drain	$I_L = 0$ , $V_{IN} = 30V$		2.3	3.5	mA
Long Term Stability			0.1		%/Khr

Note 3. Applies for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

Note 4. These parameters, although guaranteed, are not tested in production.

CHARACTERISTIC CURVES

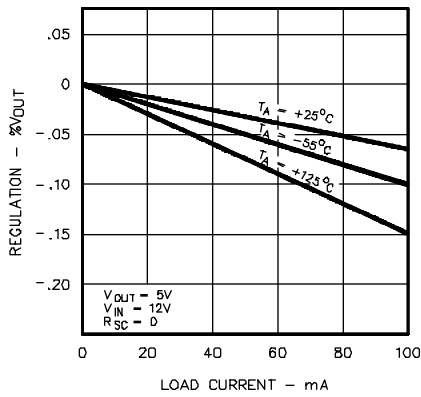


FIGURE 1. LOAD REGULATION

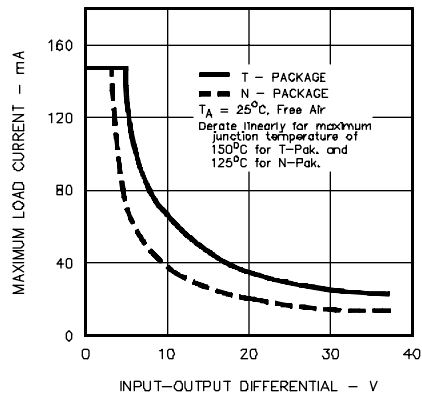


FIGURE 2. MAXIMUM LOAD CURRENT

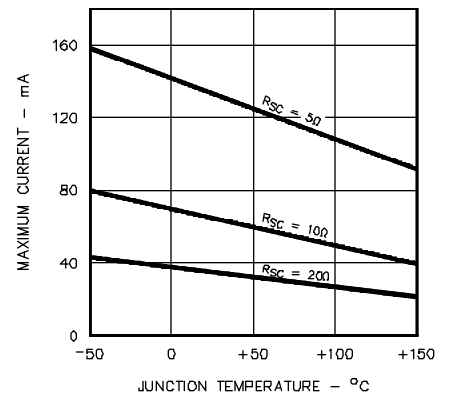


FIGURE 3. CURRENT LIMITING CHARACTERISTICS

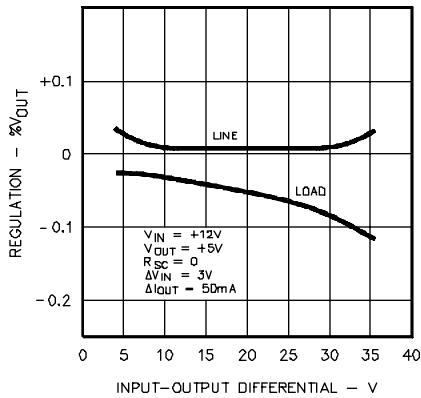


FIGURE 4. REGULATION VS. INPUT-OUTPUT VOLTAGE REGULATION

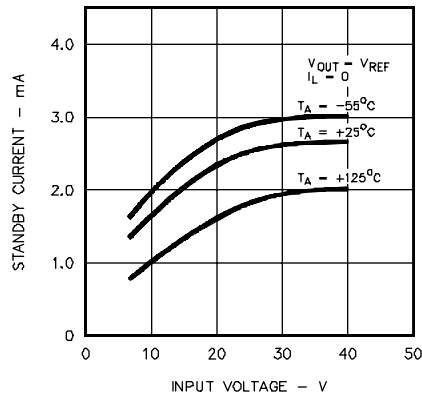


FIGURE 5. STANDBY CURRENT DRAIN

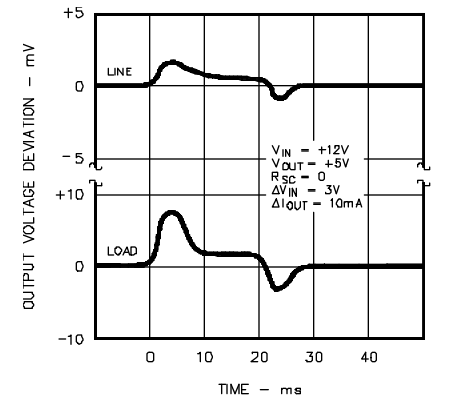


FIGURE 6. TRANSIENT RESPONSE

APPLICATION INFORMATION

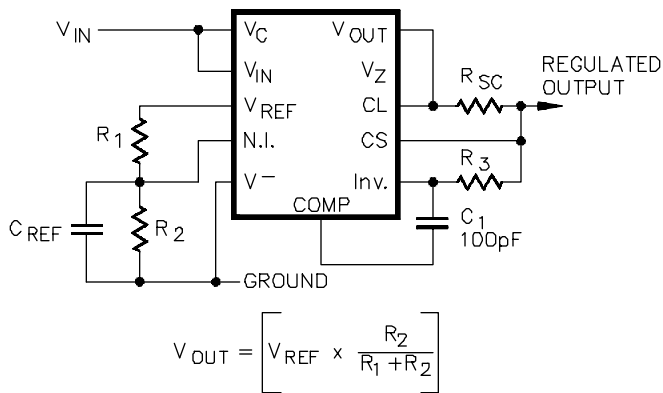


FIGURE 7 - BASIC LOW VOLTAGE REGULATOR  
 $V_{OUT} = 2\text{V TO } 7\text{V}$

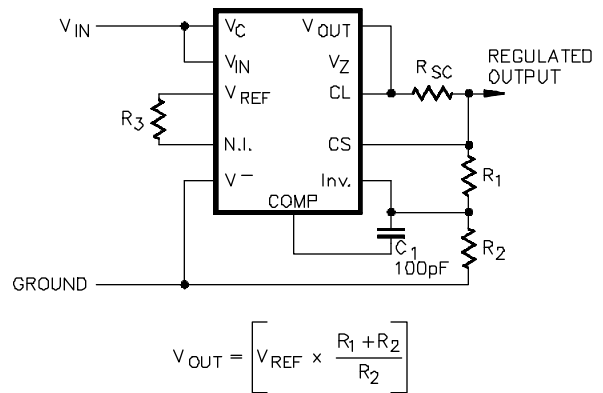


FIGURE 8 - BASIC HIGH VOLTAGE REGULATOR  
 $V_{OUT} = 7\text{V TO } 37\text{V}$

**APPLICATION INFORMATION** (continued)

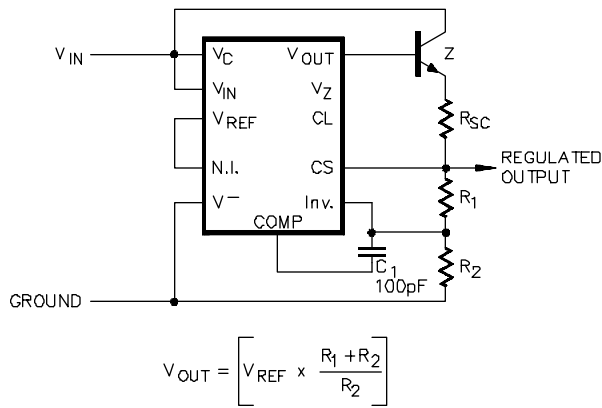


FIGURE 9 - HIGH CURRENT REGULATOR  
EXTERNAL NPN TRANSISTOR  $I_L = 1.0A$

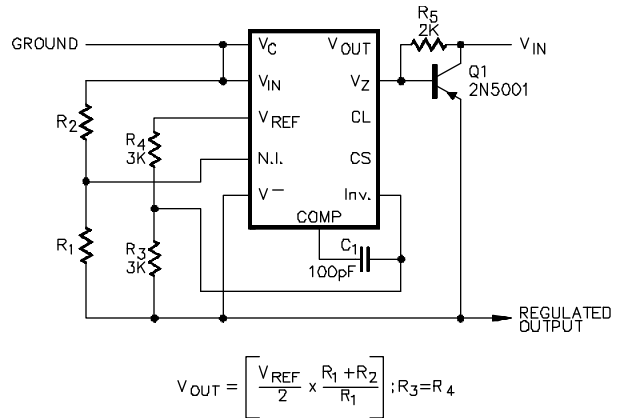


FIGURE 10 - NEGATIVE VOLTAGE REGULATOR

**CONNECTION DIAGRAMS & ORDERING INFORMATION** (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
14-PIN CERAMIC DIP J - PACKAGE	SG723J/883B JAN723J SG723J	-55°C to 125°C -55°C to 125°C -55°C to 125°C	
10-PIN METAL CAN T - PACKAGE	SG723T/883B JAN723T SG723T	-55°C to 125°C -55°C to 125°C -55°C to 125°C	<p>(Notes 3 &amp; 4)</p>
10-PIN CERAMIC FLAT PACK F - PACKAGE	JAN723F	-55°C to 125°C	<p>(Note 3)</p>
20-PIN CERAMIC LEADLESS CHIP CARRIER L - PACKAGE	SG723L/883B SG723L	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.  
2. All packages are viewed from the top.

Note 3.  $V_Z$  output is not available in T, F-packages.  
4. Pin 5 is connected to case.